

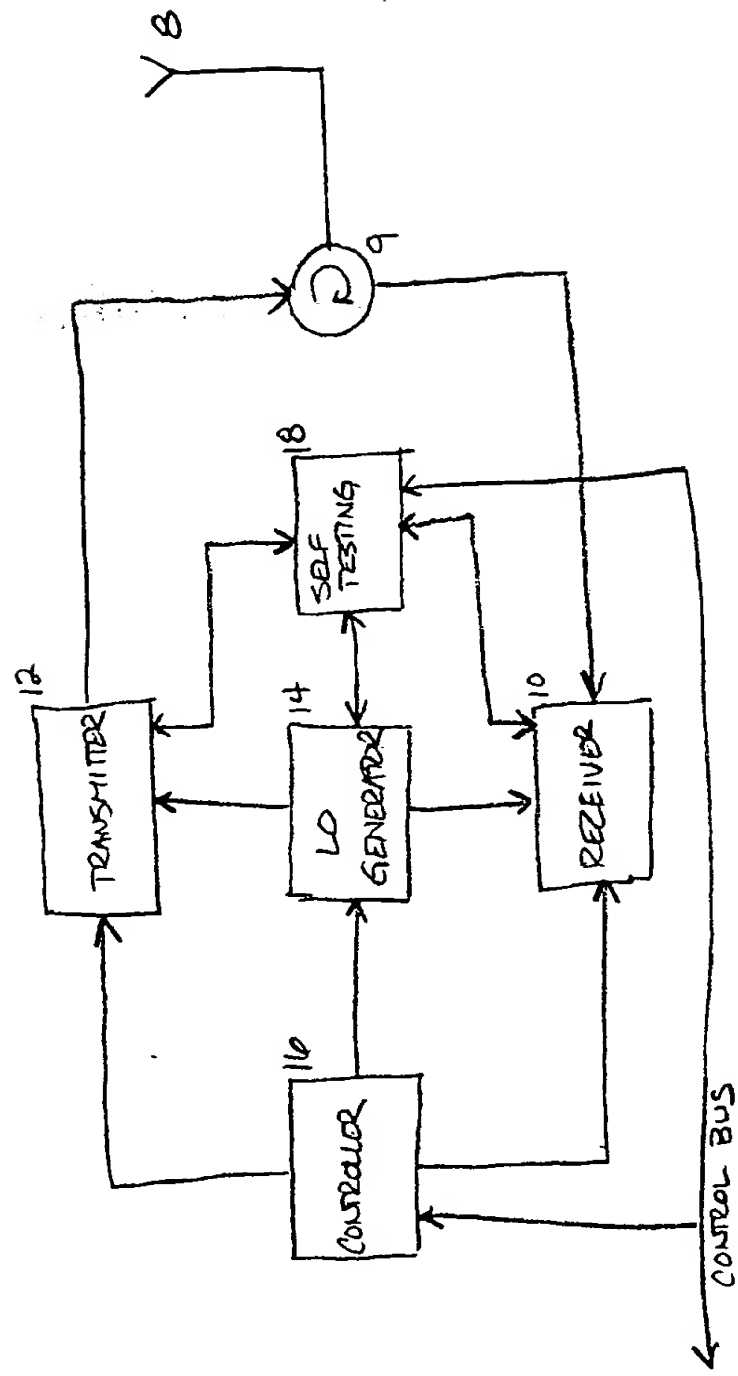
[illegible]

Fig. 1

000000 2546960

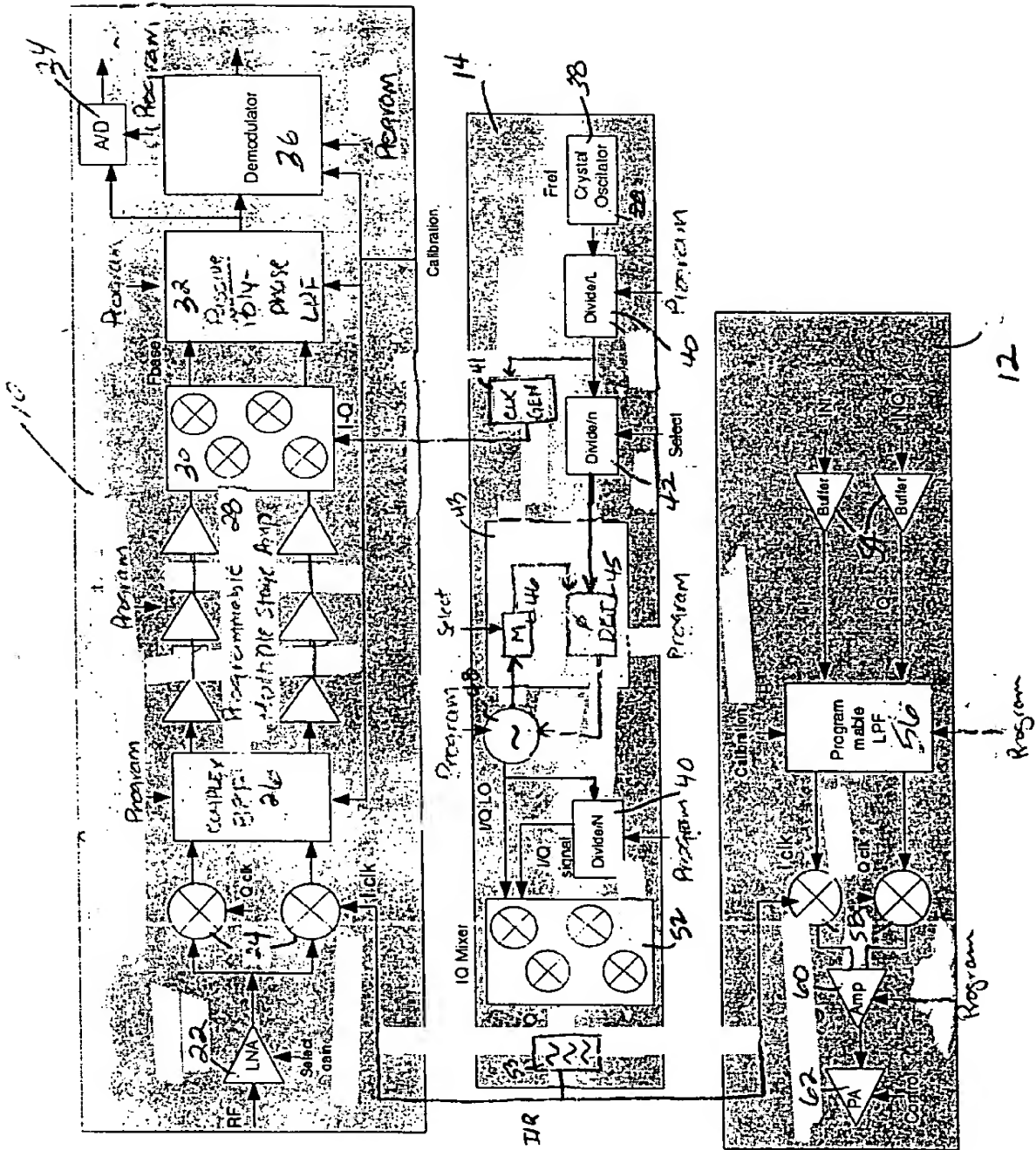


FIG. 2

000000 21554E950

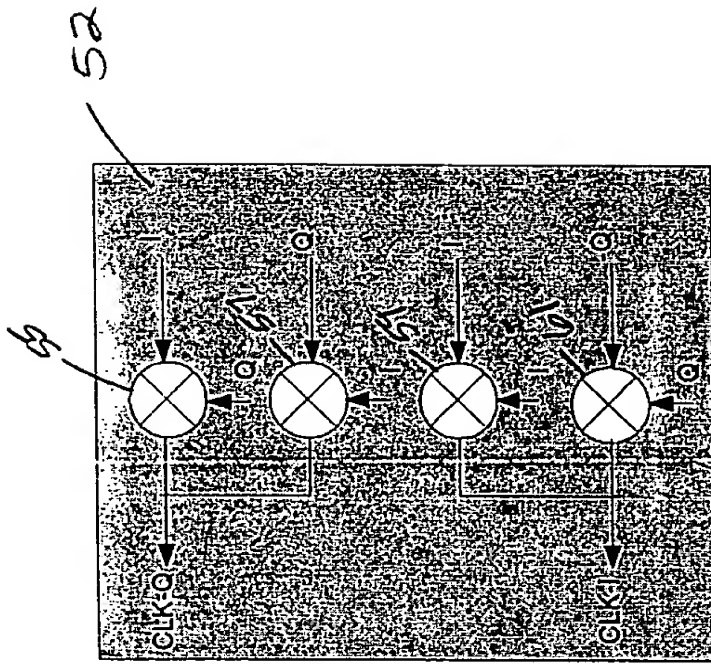


FIG. 3

**FIG. 4**

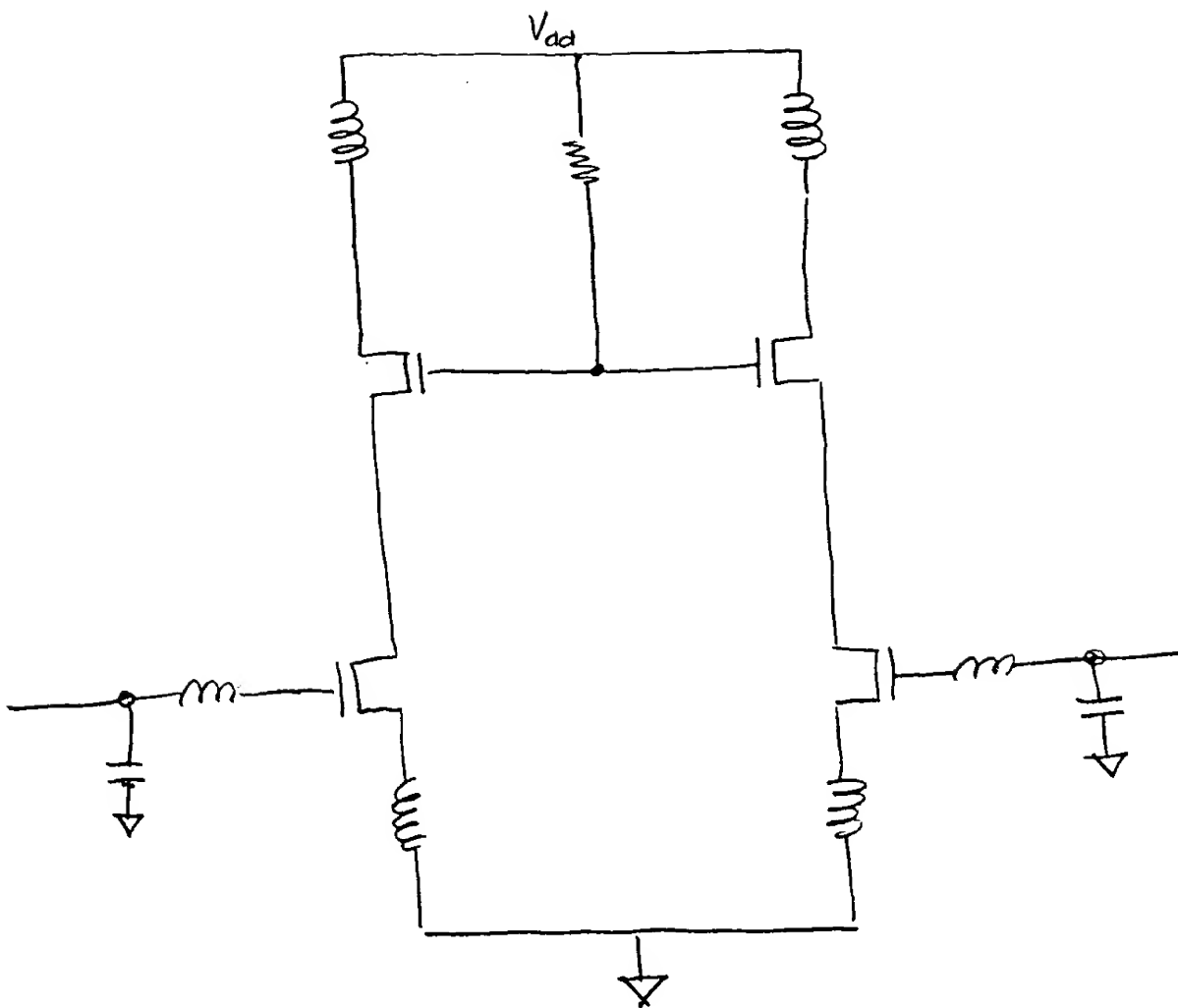


FIG. 4(a)

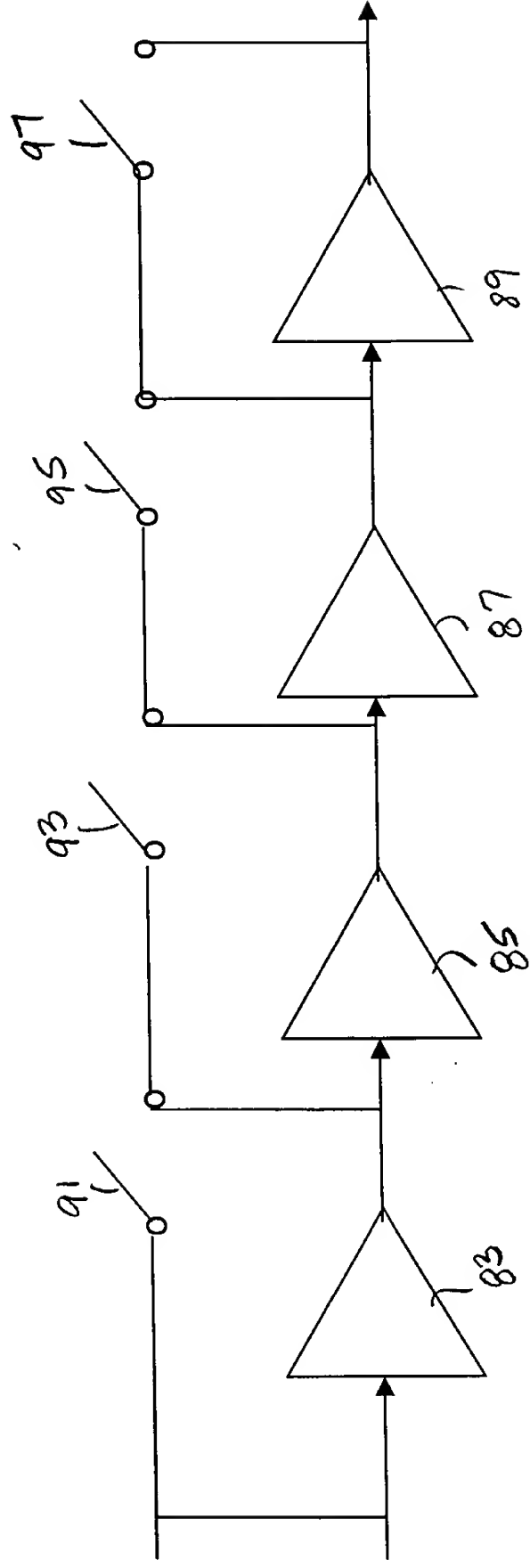


FIG. 5

09634550.000000

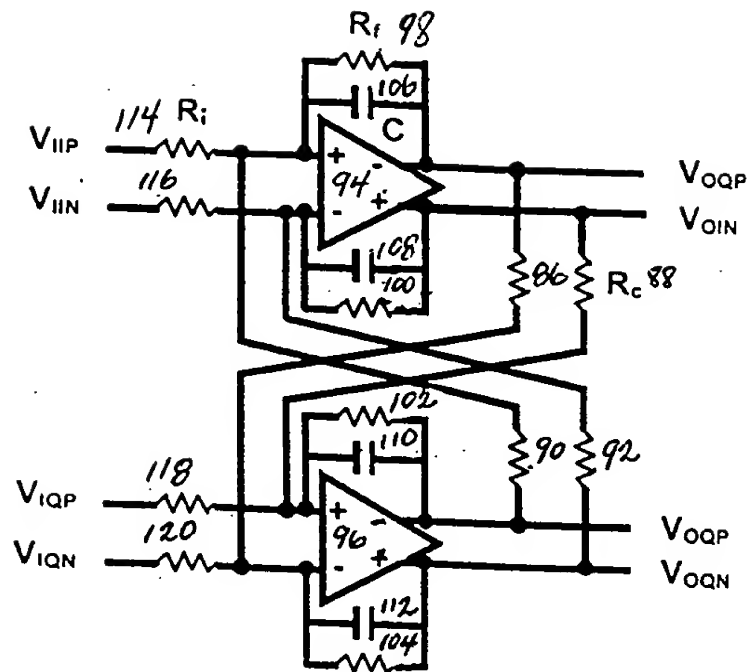


FIG. 6

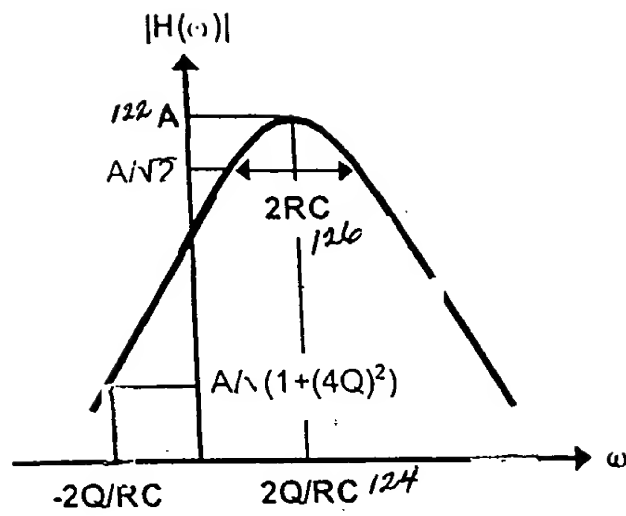


FIG. 7



Diagram for finding  $Y_i$ : A voltage source  $V$  is connected to a parallel combination of a capacitor  $C_z$  (130) and a resistor  $R_z$  (120). The output terminals are shorted to a "Virtual Ground". The current  $I$  is shown flowing into the short. The input admittance is given as  $Y_i = I/V$ .

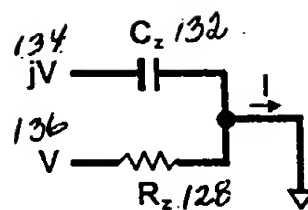


FIG. 9

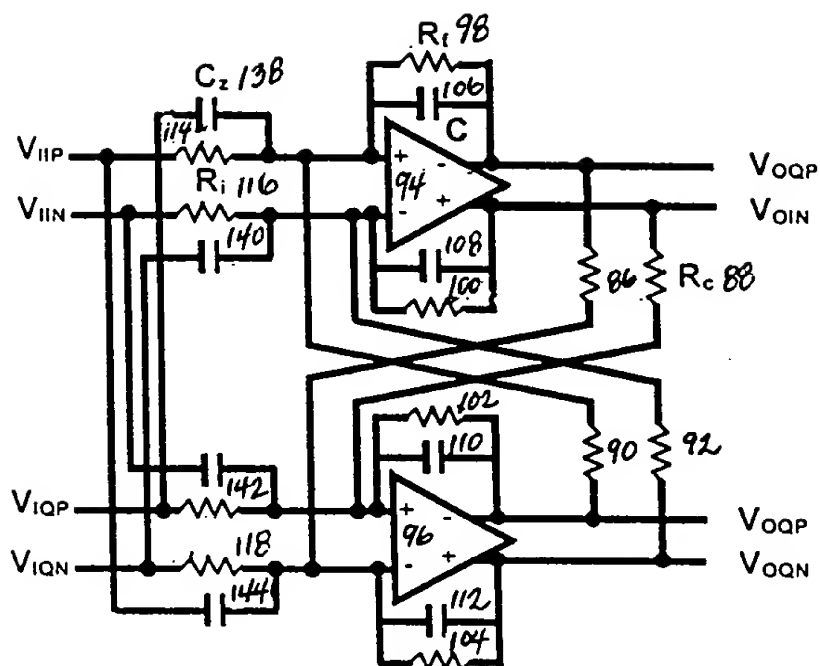
[illegible]

FIG. 10

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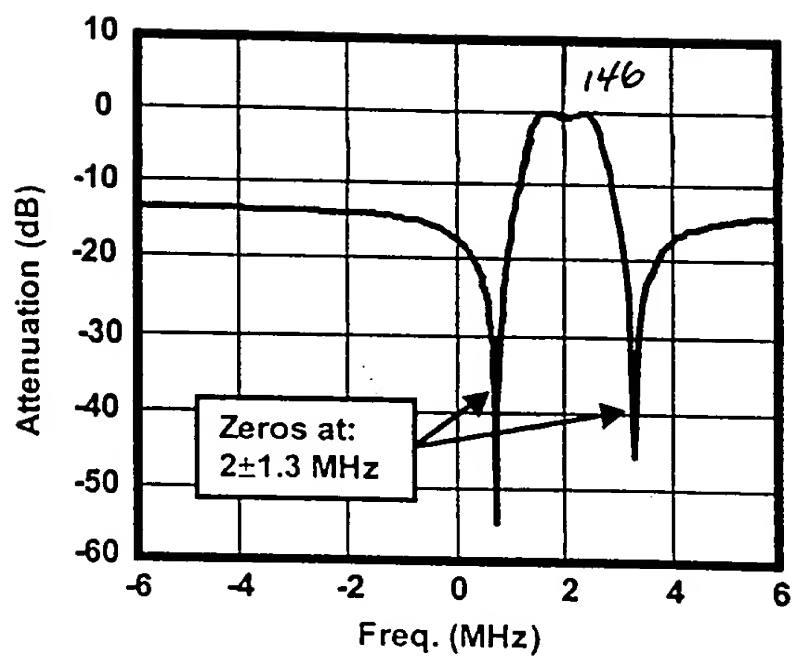


FIG. 11

Diagram of a 4-bit parallel adder using four 1-bit full adders. The inputs are  $A_4, A_3, A_2, A_1$  and  $B_4, B_3, B_2, B_1$ . The outputs are  $S_4, S_3, S_2, S_1$ . The carry chain is shown as  $C_n/2, C_n/2, C_n/4, C_n/8, C_n/16$ .

FIG. 12(b)

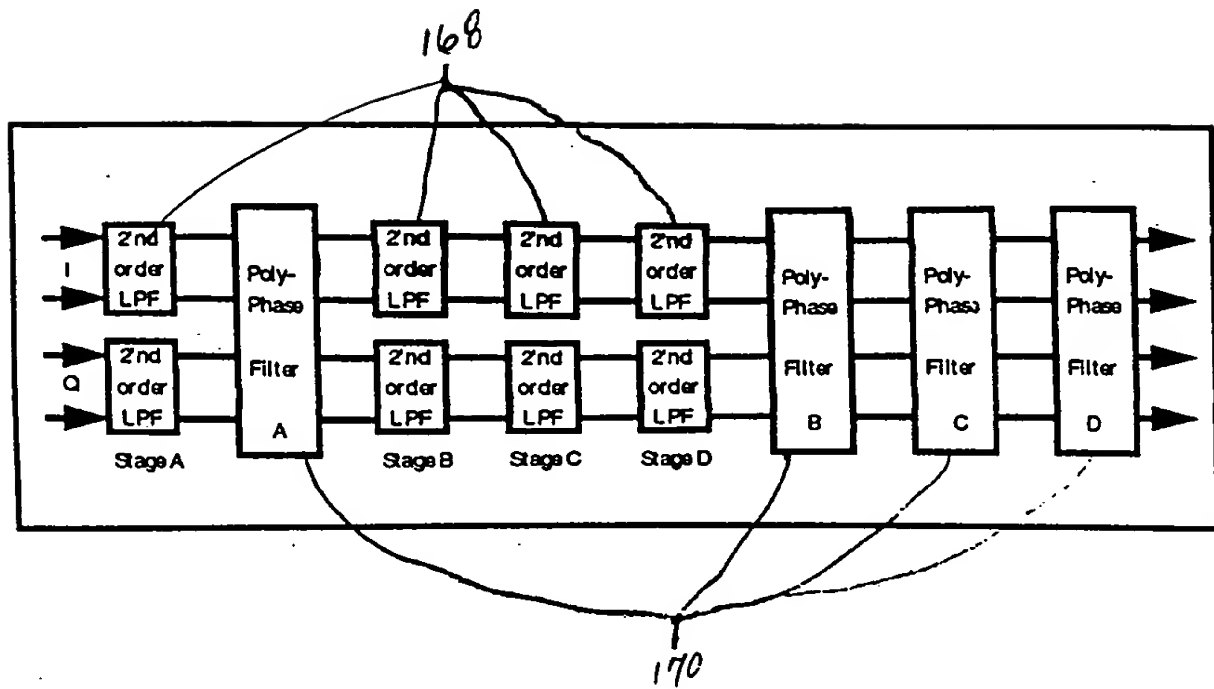
[illegible]

FIG. 13

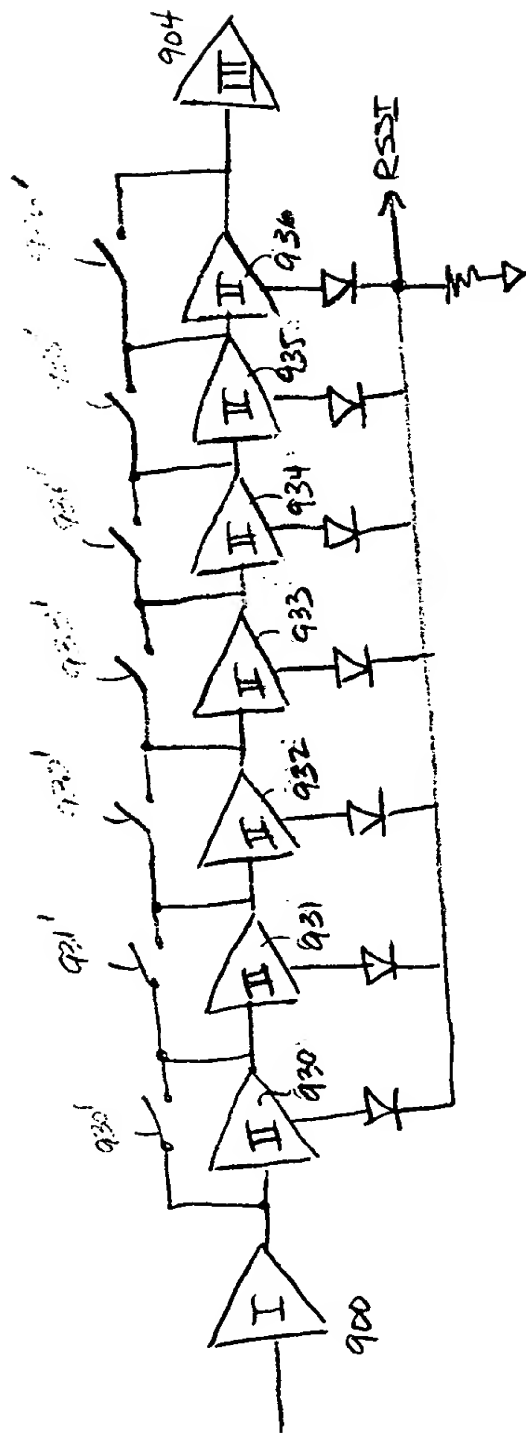


FIG. 14

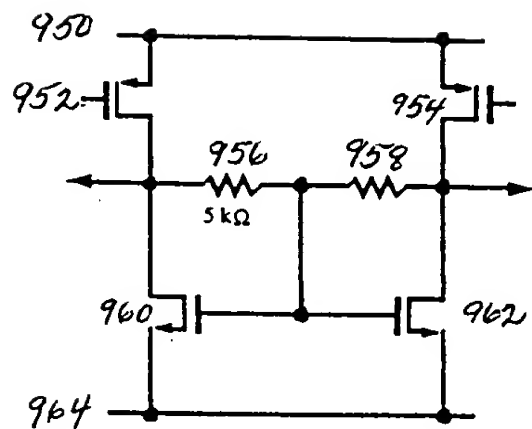
[illegible]

FIG. 15

FIG. 16(a)



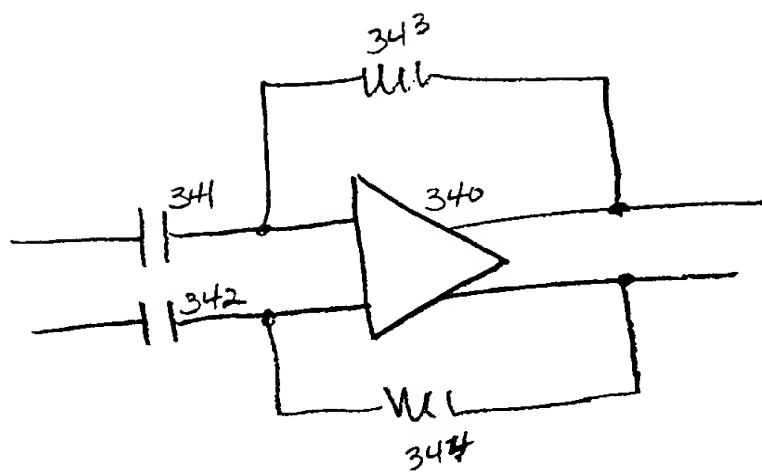


FIGURE 22



FIG. 17(a)

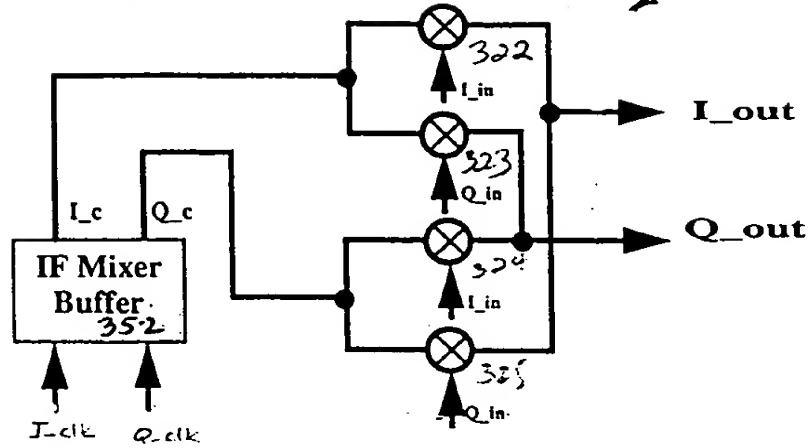


FIG. 17(b)

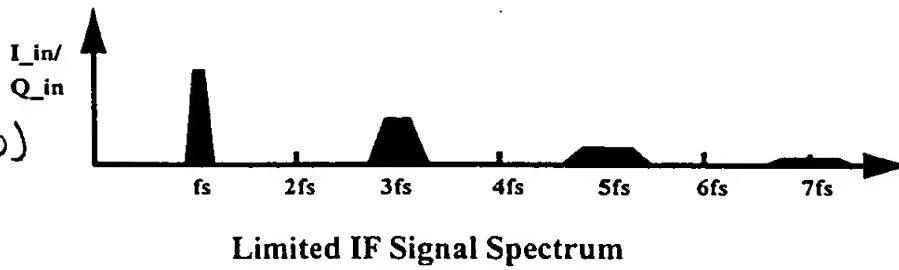


FIG. 17(c)

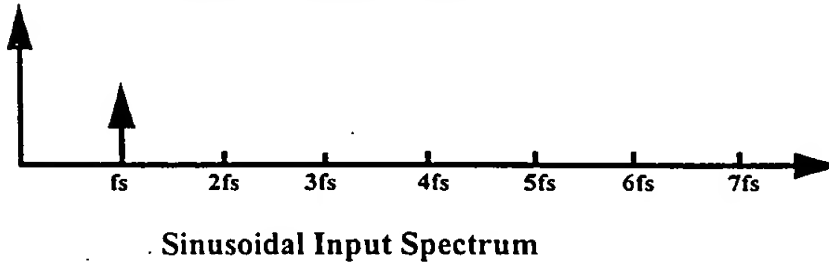


FIG. 17(d)

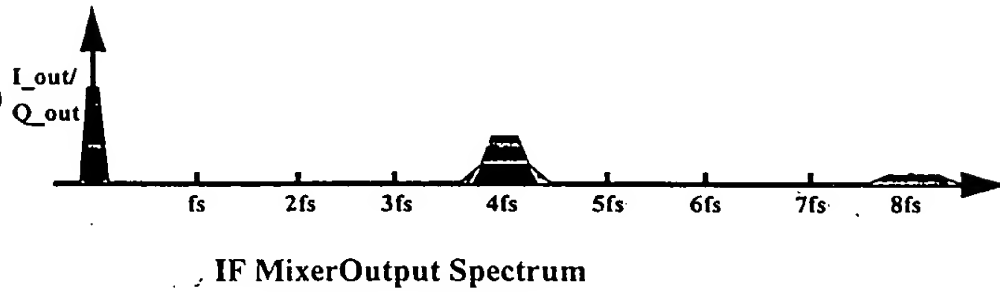


FIG. 18

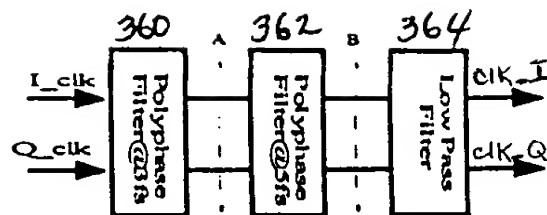


FIG. 19(a)

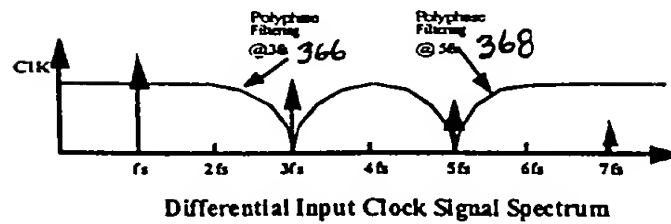


FIG. 19(b)

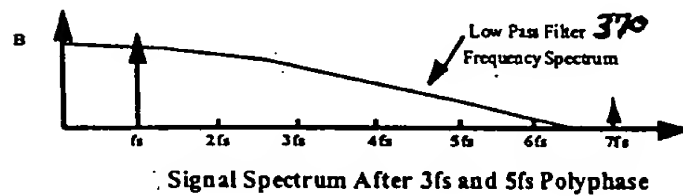
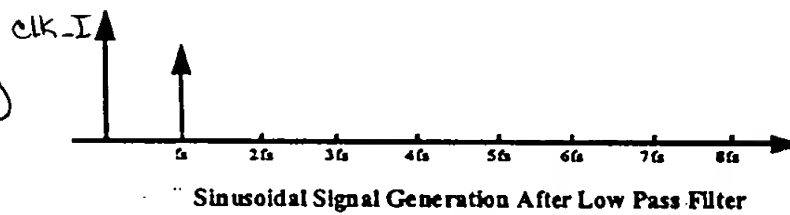
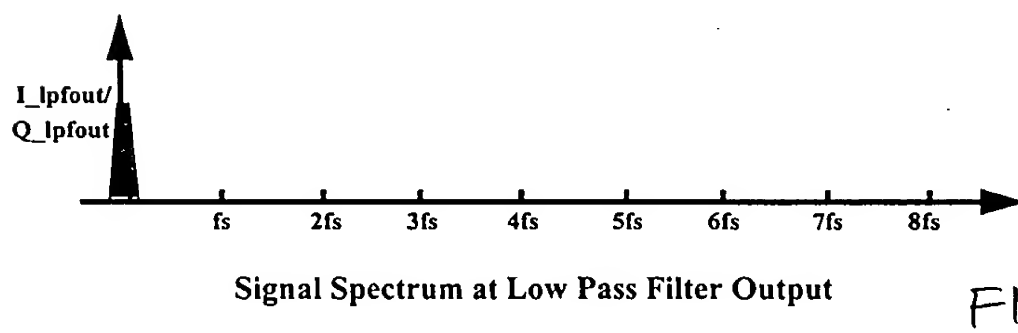
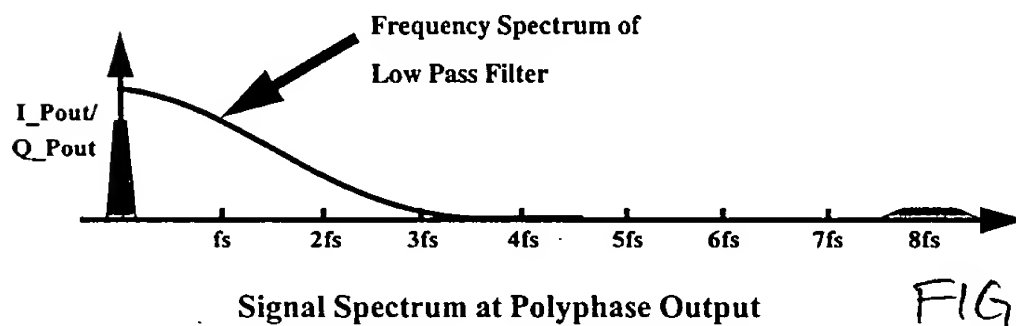
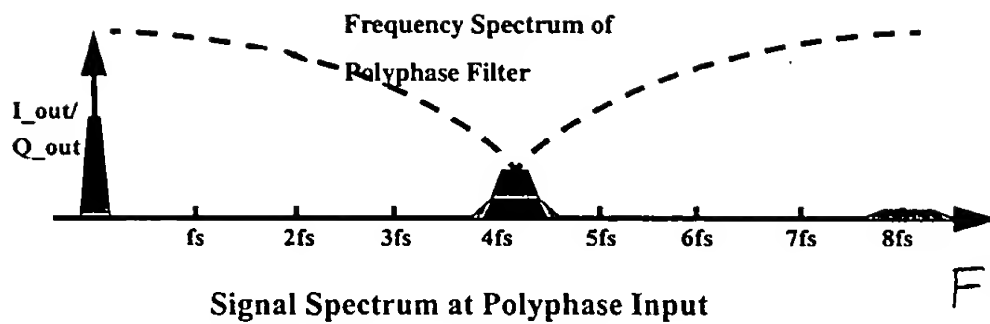


FIG. 19(c)



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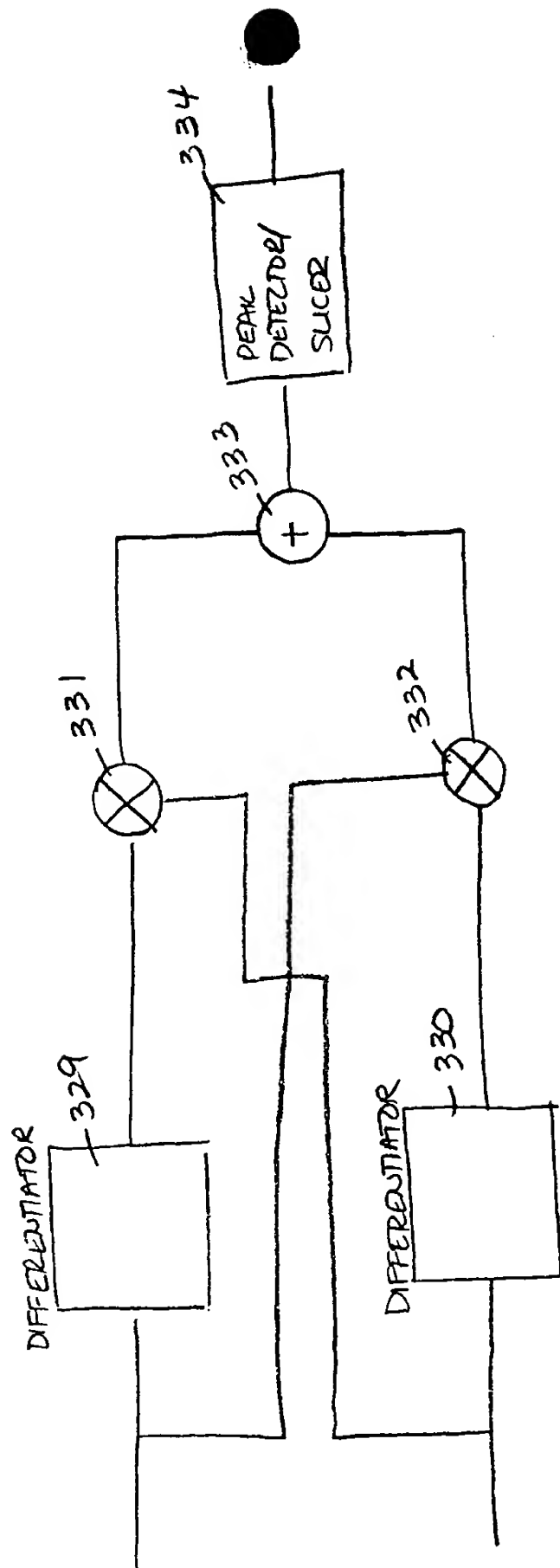
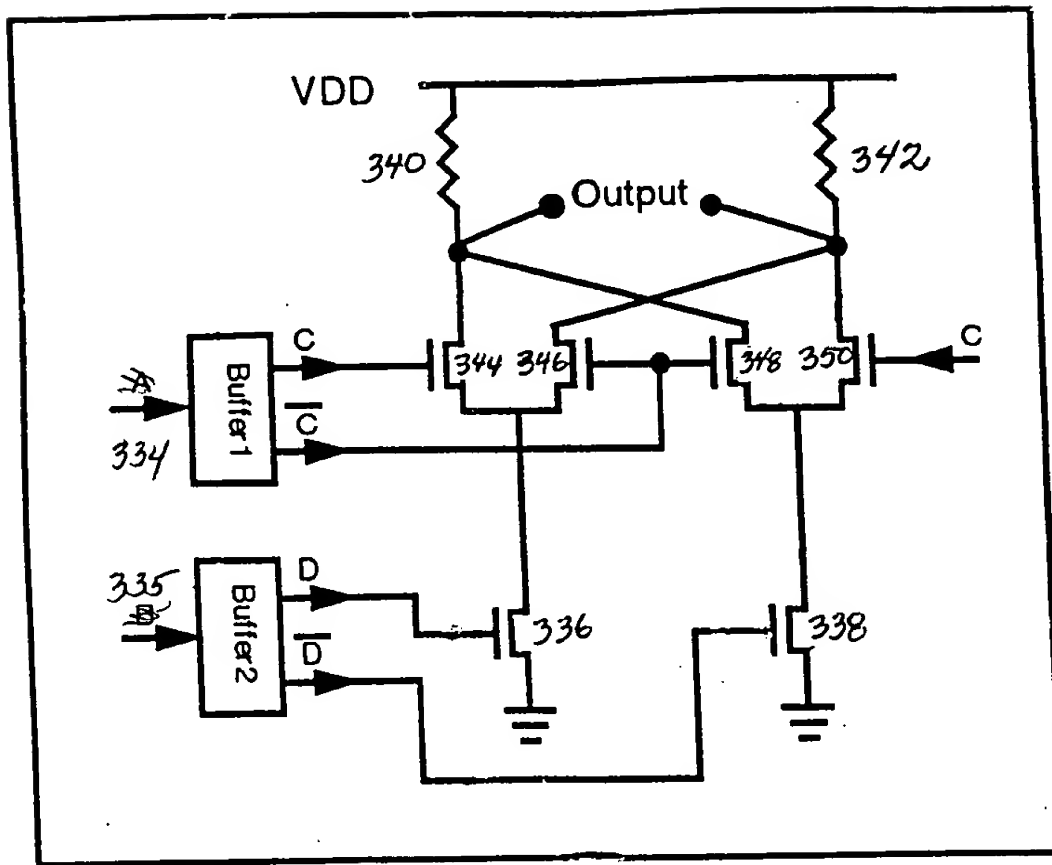


FIG. 21

FIG. 23



# C O N T E N T S

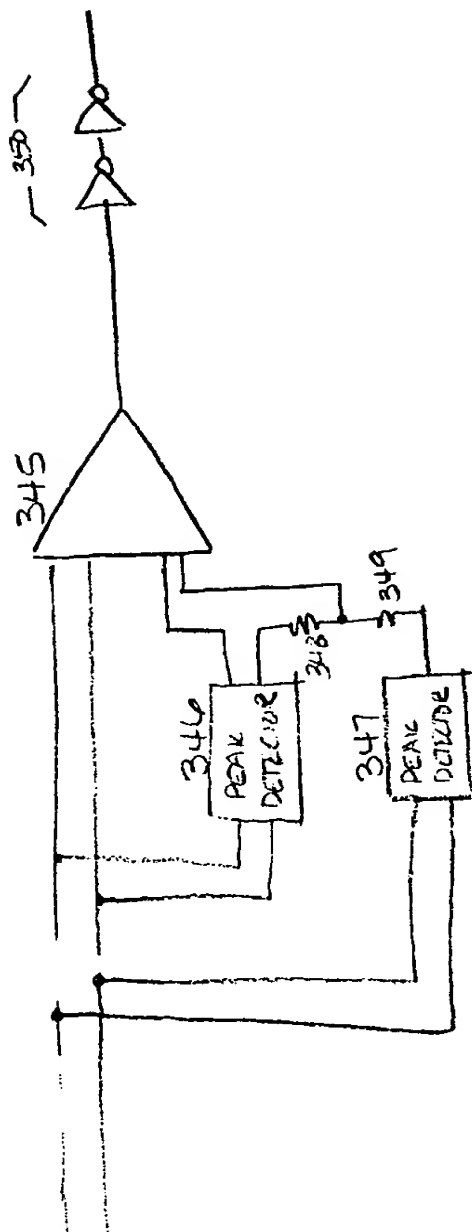


FIGURE 24



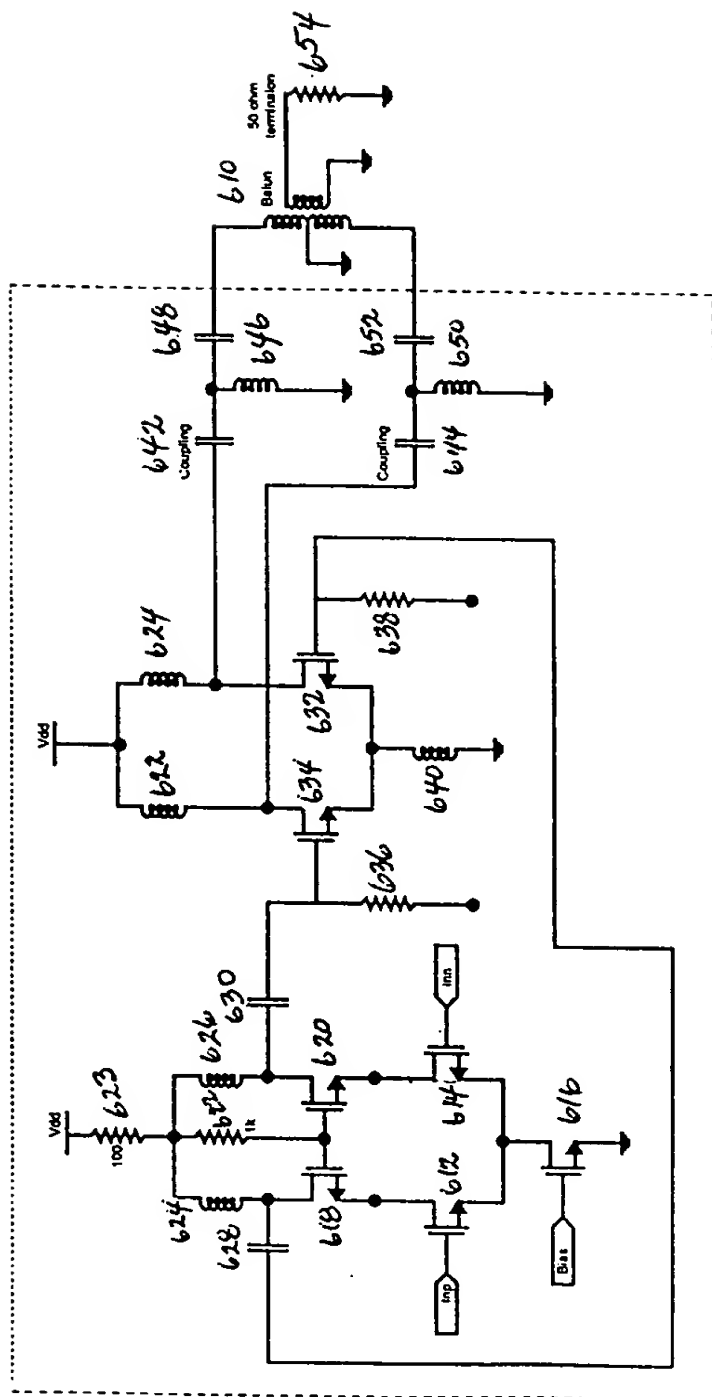


FIG. 25

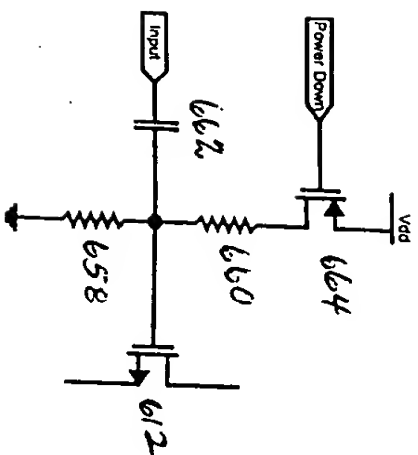


FIG. 26(a)

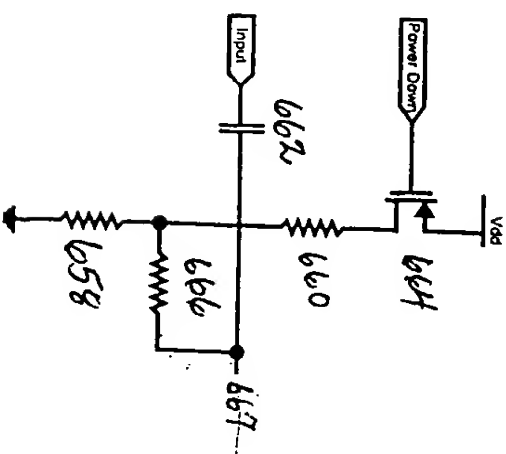


FIG. 26(b)

FIG. 27

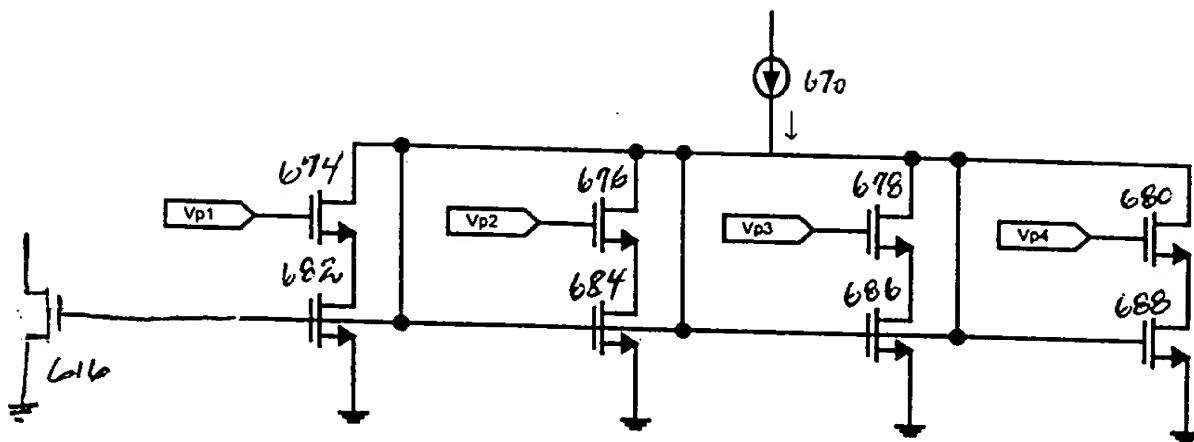
[illegible]

FIG. 28



000000 " 000000

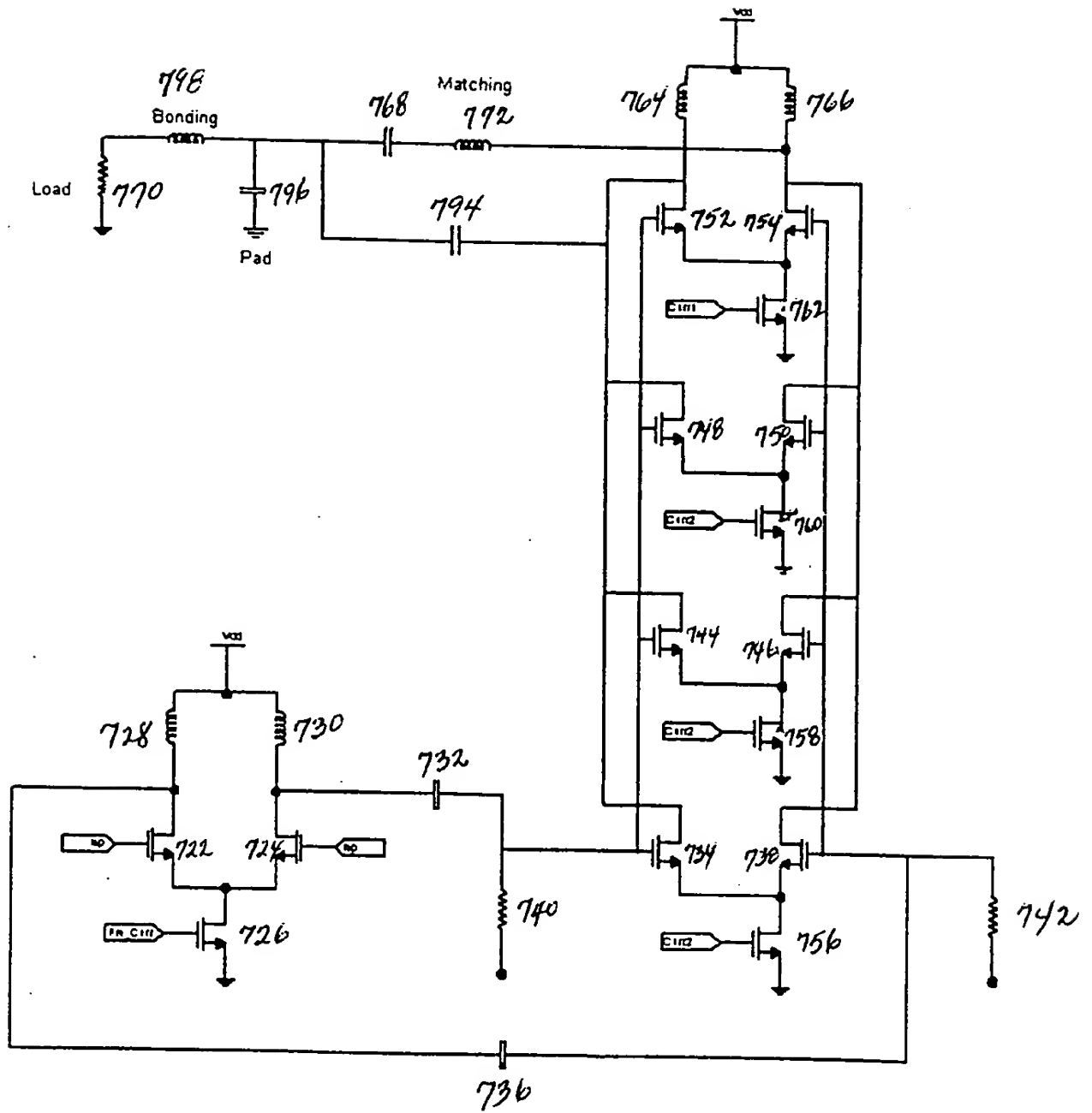


FIG. 30



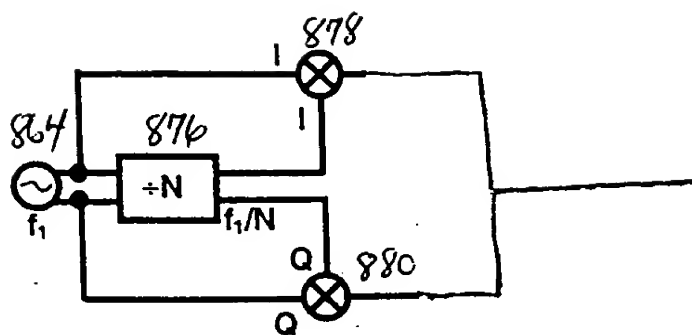


FIG. 32



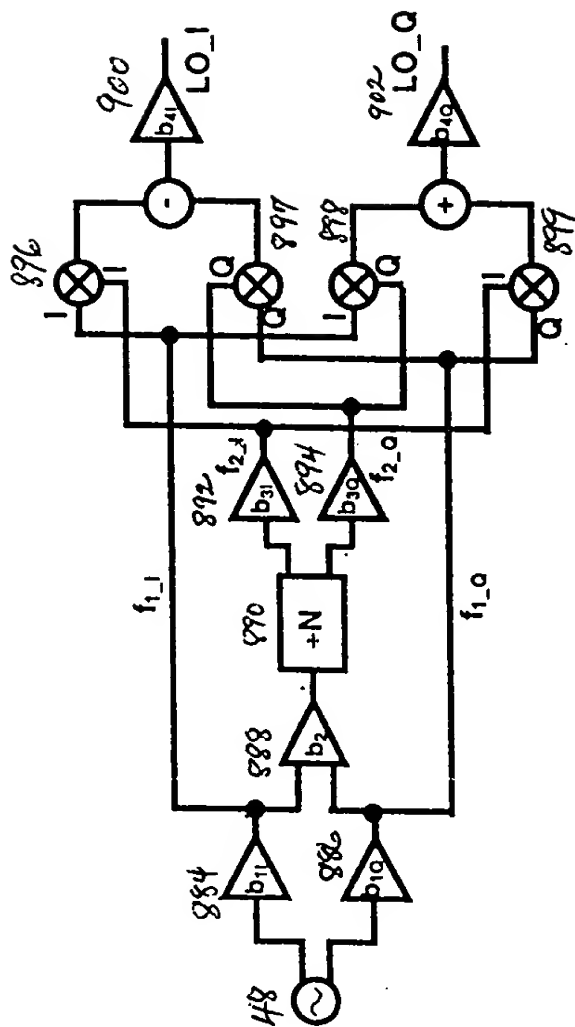


FIG. 33



FIG. 33(a)

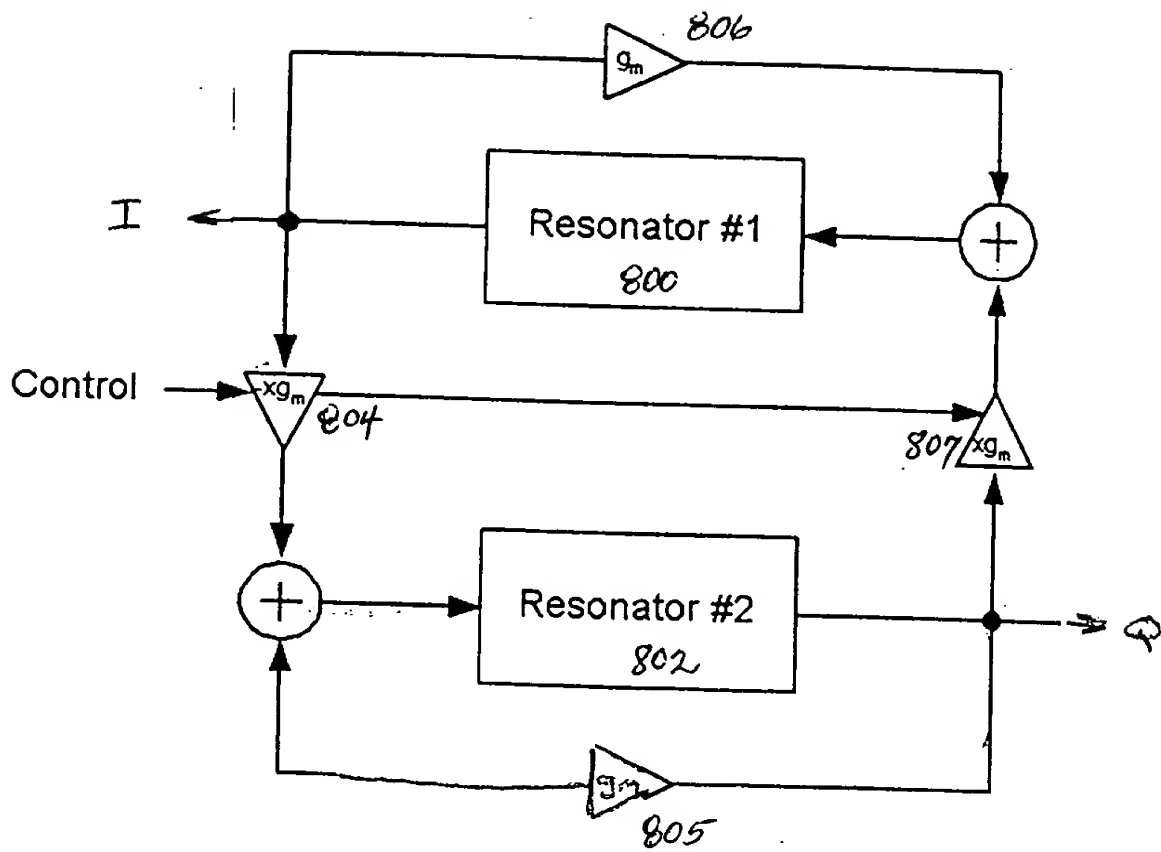
[illegible]

FIG. 34

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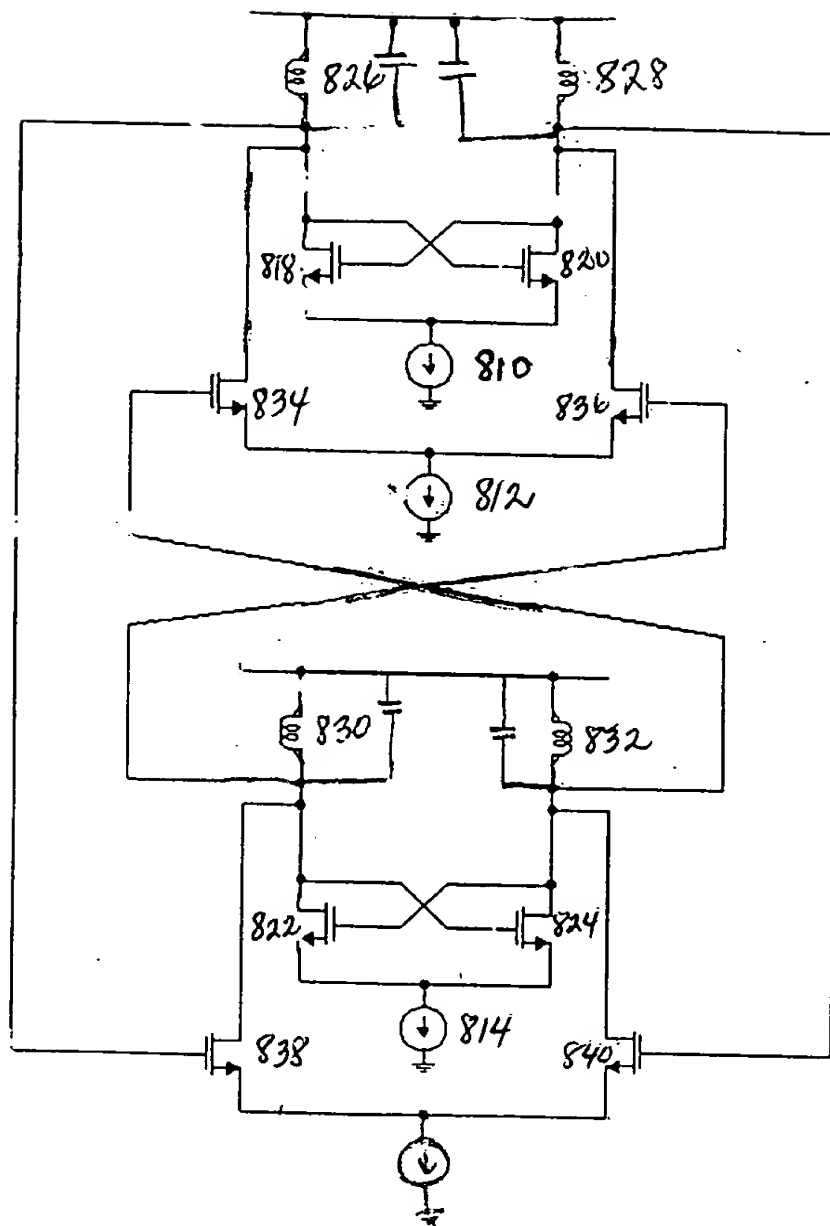


FIG. 35

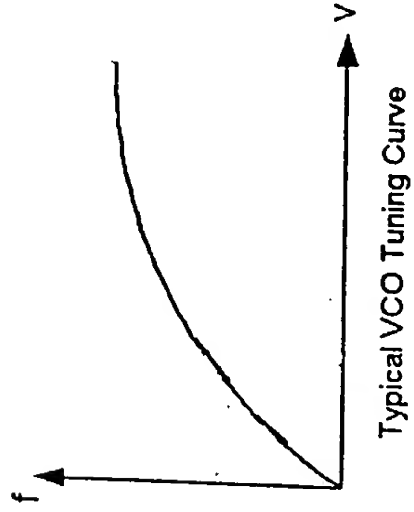


FIG. 36(a)

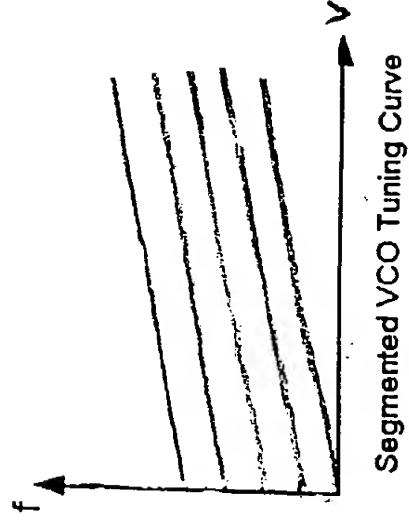


FIG. 36(b)

1. The first step is to identify the problem. This involves understanding the current situation and the goals that need to be achieved.

FIG. 37(a)

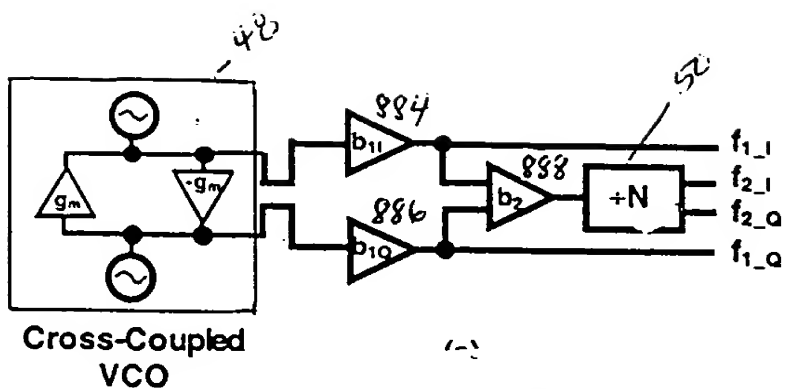
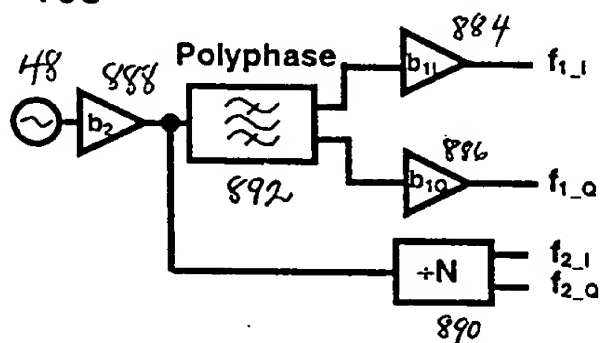


FIG. 37(b)



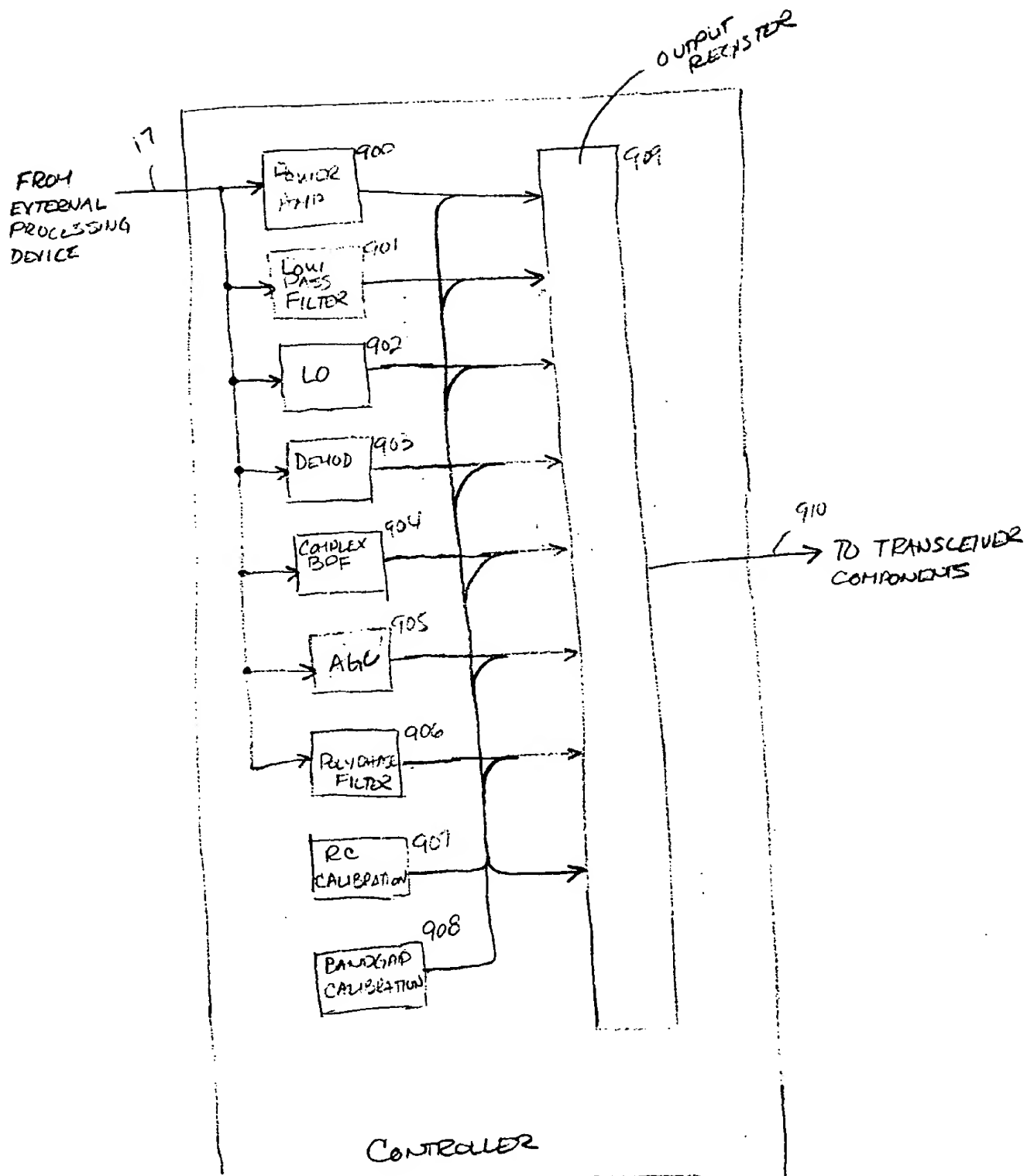
[illegible]

FIGURE 38

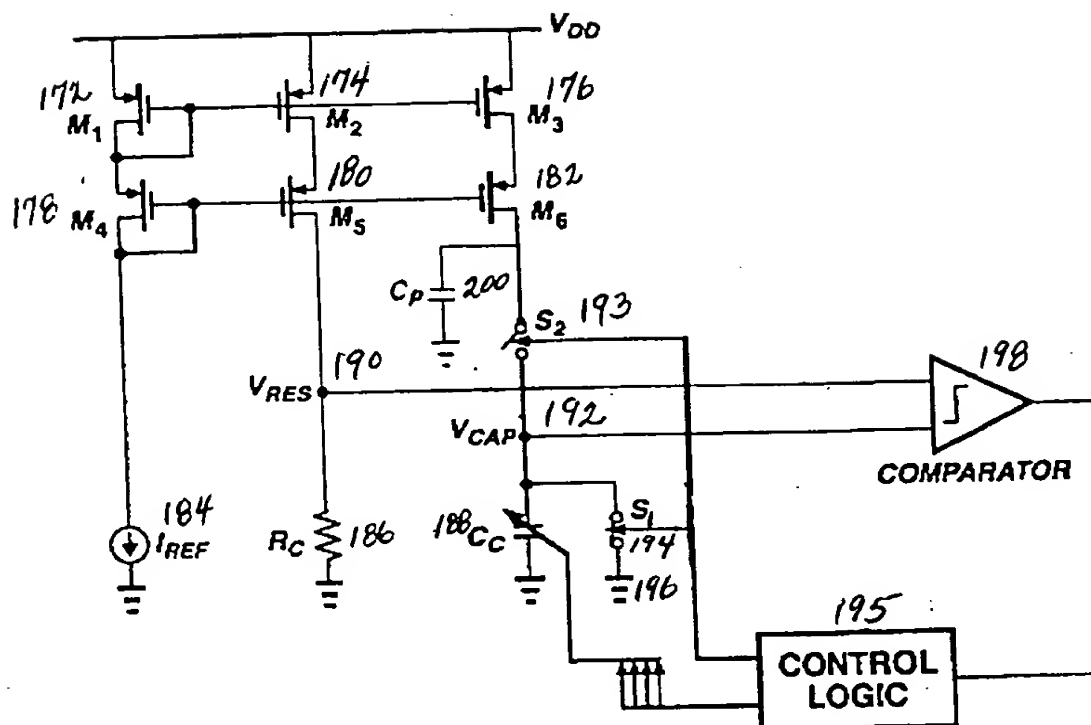
[illegible]

FIG. 39



FIG. 1 is a block diagram of a PLL circuit. The input signal  $X_{IN}$  is split into two paths. One path goes through a divider (280) to the **POLYPHASE A** block (282). The other path goes through a divider (281) to the **POLYPHASE B** block (282). The outputs of these blocks are  $X_A$  and  $X_B$ , which are fed into the **RSSI** (Reference Signal Sensing Interface) block (284). The **RSSI** block has two outputs, 286 and 288, which are fed into the **CONTROL LOGIC** block (286). The **CONTROL LOGIC** block also receives a clock signal  $CK$  (250 kHz) and outputs a control signal  $<C_A>$  to the **POLYPHASE A** block and a control signal  $<C_B>$  to the **POLYPHASE B** block.

FIG. 40

1. The first part of the paper is devoted to the study of the properties of the function  $f(x)$  defined by the equation  $f(x) = \int_0^x f(t) dt$ . It is shown that  $f(x)$  is a continuous function and that it satisfies the functional equation  $f(x+y) = f(x) + f(y)$ . The function  $f(x)$  is also shown to be differentiable and its derivative is found to be  $f'(x) = f(x)$ . This implies that  $f(x) = Ce^x$  for some constant  $C$ . The value of  $C$  is determined by the initial condition  $f(0) = 1$ , which gives  $C = 1$ . Therefore, the function  $f(x)$  is the exponential function  $f(x) = e^x$ .

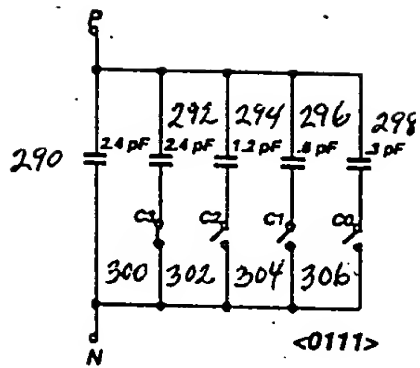
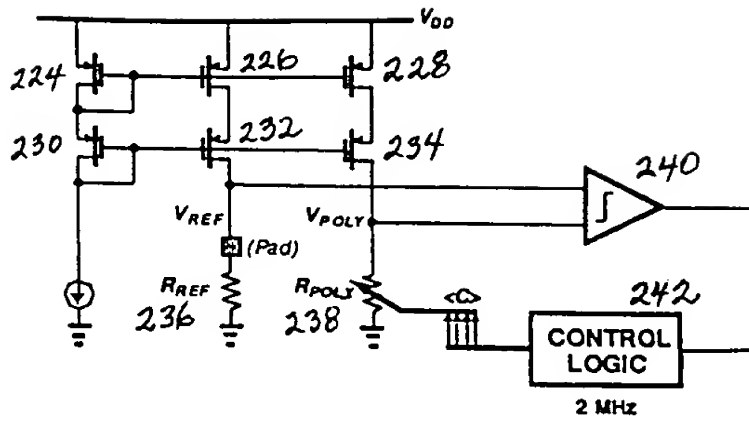


FIG. 41

FIG. 42



09634530.030300

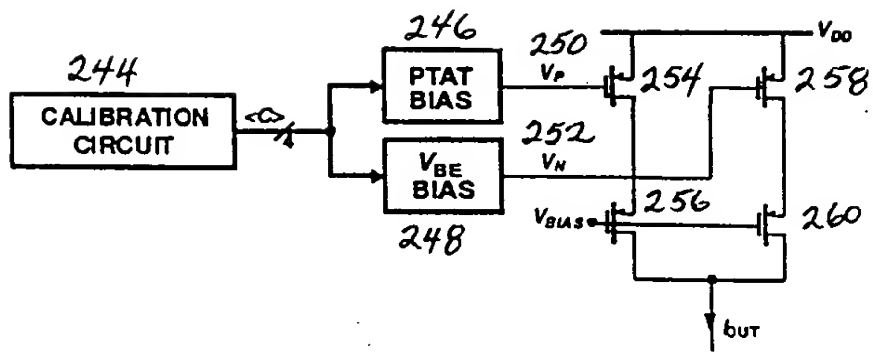


FIG. 43

000000 254950

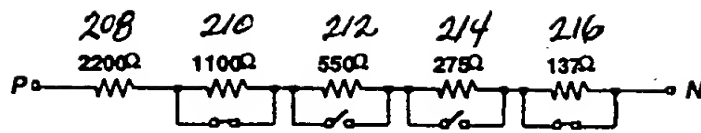


FIG. 44

FIG. 45



